

Performance Analysis of a Fault-Tolerant Crossbar Molecular Switch Memory Demultiplexer

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Abstract

Nanoscale elements are fabricated using bottom-up processes, and as such they are prone to high levels of defects. Defect-tolerance will play a crucial role in the realization of practical nanoscale devices. In this paper we investigate the performance impact of combining a molecular switch junction with an ECC demultiplexer to allow for enhanced fault-tolerance. The results indicate that the molecular switch junction, which adds redundancy to the address lines, aids in reducing the delay as the redundancy increases. Further, the probability analysis also indicates that the fault tolerance improves with the combined scheme.

I. Introduction

Hybrid technologies, where CMOS and nanotechnologies are integrated to constitute devices, are seen as the natural progression on the pathway to realizing practical nanoscale devices. Nanowires (NW) and Carbon Nanotubes (CNT) are emerging as the building blocks for future nanoelectronics devices. Methods now exist to better control the diameter, aspect ratios, pitch and regularity of NWs and NW arrays [1]. A hybrid molecular crossbar RAM has already been demonstrated by Chen et al [2]. The molecular RAM consists of an 8×8 crossbar of NWs that implement a 4×4 molecular RAM and a row and column demultiplexer.

It is expected that the defect rate of nano-components will be inferior to that of CMOS components. Defect rates as high as 15% have been reported for crossbar molecular switch memories [2]. Thus, defect-tolerance is crucial to realizing practical nanoelectronic devices.

An Error-Correction Code (ECC) scheme, implemented via the incorporation of redundancies into the micro-wire interconnects of the molecular RAM demultiplexer, has been proposed as a means of achieving defect-tolerance in demultiplexers [4]. In this paper we investigate the performance penalties of

implementing ECC defect-tolerance in molecular RAM demultiplexers. Performance analysis as described in this work pertains to the relative delay experienced by the demultiplexer from the time of signal input to the time the signal reaches the output of the selected NWs. The delay of different demultiplexer sizes, for varying degrees of ECC is investigated. The goal of this effort is to analyze the cost-benefit relationship between defect tolerance and delay.

The ECC defect-tolerant scheme has been simulated using the Synopsys CAD tool, Saber Sketch. A transient model of the circuit, which incorporates the electrostatic and quantum capacitance of the NWs and micro-wires is discussed. Furthermore, an analysis of the relative delay incurred by implementing redundancies in the NWs of the ECC defect-tolerant demultiplexer decoder is presented. The addition of redundant NWs will allow for defects in the NW domain. This scheme will aid in the enhancement of the overall defect-tolerance probability of the molecular RAM demultiplexer. By virtue of the architecture of this scheme, multiple molecular switch junctions will be created at each micro-wire/NW intersection, so that defective molecular switch junctions can be tolerated. This work has shown that by including redundant SWNT bundles in the AND gate address line of a nanomemory demultiplexer implemented with ECC, delay performance can be further improved. Further, fault-tolerance for the large array of defect probabilities is improved.

II. Defect-Tolerant Crossbar Demultiplexers

Demultiplexers represent one of the most vital components of a nanoscale memory. Demultiplexers are able to control 2^i output lines using only i input signals. Its function in a crossbar nanomemory is to select a specific address line -to be read or written- while keeping other unselected address lines off. Nanoelectronic memories utilize a hybrid of CMOS and nanoelectronic components to implement a crossbar

memory decoder. The role of the demultiplexer is essential to the reliability of the crossbar nanomemory. It is located at the interface of the CMOS circuitry which means that a failure in the demultiplexer will have a trickle down effect on the rest of the crossbar nanomemory device.

Molecules sandwiched between intersecting NWs, constitute the “ON” and “OFF” switches of the nanoelectronic device. Molecular switches exhibiting properties such as coulomb blockade, current rectification, Negative Differential Resistance (NDR) and bistable switching, have already been demonstrated [7,8,9,10,11]. The implementation of feasible molecular switches is being impeded by obstacles, such as the selection of adequate bistable molecules and the high resistance encountered at the metal-molecule-metal interface.

Fig 1. Illustrates a demultiplexer laid out in a crossbar configuration which controls a 4×4 crossbar nanomemory. Two signals, A0 and A1, which drive four micro-wires (vertical wires) signal lines, have molecular intersecting junctions with the NW address lines as illustrated by the resistor junctions. The output address lines can be thought of as having an AND gate functionality. Hence, a NW address line can only be selected if its two input signals are high or “1”.

A. Defect-tolerant ECC Demultiplexers

As mentioned previously, a defect-tolerant scheme that utilizes an ECC methodology has been proposed [4]. This scheme is implemented by widening the n bit address of the demultiplexer to include redundant error correcting bits. The expanded address is derived by computing the minimum distance d between adjacent addresses. This distance is defined as the hamming distance, which refers to the number of different address bits in two equivalent address lengths. The Hamming distance is computed by an encoder to guarantee efficient code selection. Up to $(d - 1)$ faults can be tolerated by this scheme.

The ECC demultiplexer is implemented using both CMOS and nano circuits. The CMOS circuit is comprised of the selecting micro-wire interconnects bits, input signal driver, $(i - r)$ XOR gates and r inverters, where r is the total expanded address bits. The Nano-circuit is comprised of NWs and molecular switch junctions. By adding the XOR gate, redundant bits can be added to the address bits.

Fig. 2 provides an illustration of the ECC scheme with the enhancing molecular switch junction scheme. Redundant NWs is given at each of the address lines. This combined scheme targets stuck-open defects resulting from manufacturing errors. In particular, the scheme primarily targets stuck-open faults caused by

malfunctioning molecular junctions. The combined scheme creates redundant bits for each NW by adding extra address lines to the demultiplexer circuit, thereby expanding each address line such that multiple faults can be tolerated as determined by the degree of redundancy.

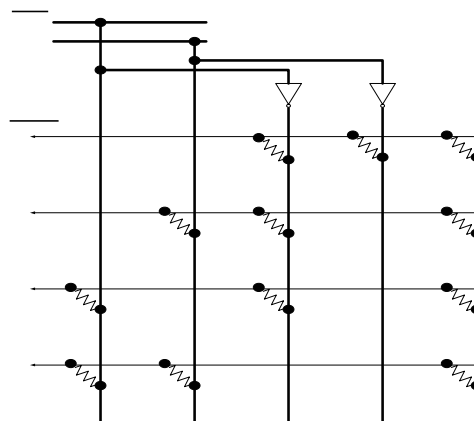


Figure 1: A molecular RAM demultiplexer that requires only m input signals to select 2^m NWs.

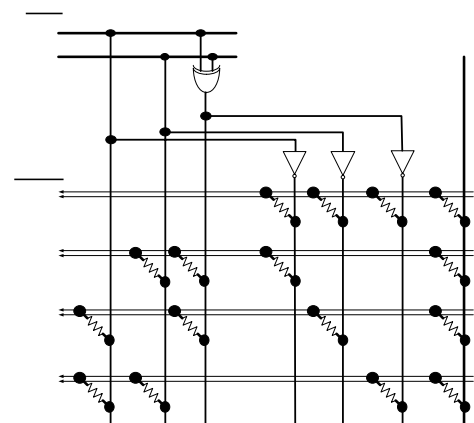


Figure 2: A molecular RAM demultiplexer with an additional EX-OR gate and inverter for ECC implementation. An additional NW is added to each row to implement the multi-switch junction scheme.

III. Nanowires and Transmission models for Demultiplexers

As interconnects shrink, they experience an increase in resistivity and become more susceptible to parasitic quantum effects. The NWs interconnects in this work have been modeled as Single Wall Metallic carbon Nanotubes (SWNT). The primary reason being, SWNTs have been extensively studied, and as such their electrical properties are better understood, more so

than most other types of NWs. SWNTs also demonstrate ballistic electron flow with electron mean paths that measure in the order of several microns [17], and have the ability to conduct large current densities.

Studies analyzing the potential use of SWNTs as transmission lines have been conducted [12, 13, 14]. Performance analysis comparing metallic SWNT and Cu for interconnect application, has also been done [13]. It has been shown that SWNT bundles have a better performance than individual SWNT interconnects [13, 17]. The electrical characteristics of SWNTs have been extensively studied.

A. SWNT Transmission line Model

In this work, interconnects are modeled as bundle of ballistic SWNTs. The details of the various properties of SWNTs are given in the following subsections

i. Inductance

The inductance of SWNTs has been computed in [15, 16]. For the case of a 1-dimensional system, the kinetic inductance per unit length of a SWNT is given by the equation below:

$$L_k = \frac{\hbar}{2e^2 v_f} \quad (1)$$

where \hbar is Planks constant and $v_f (\approx 8 \times 10^5 \text{m/s})$ is the Fermi energy of graphene. When computed $L_k = 16 \text{ nH}/\mu\text{m}$, which is the value utilized in our SWNT transmission line model.

ii. Capacitance

Parallel SWNT interconnects experience two distinct forms of capacitance [14, 15]. The first form of capacitance is a coupling electrostatic capacitance C_{ES} , given by the equation below:

$$C_{ES} = \frac{2\pi\epsilon}{\ln(h_g/d)} \quad (2)$$

where h_g is the height displacement of the SWNT above the ground plane substrate (illustrated in fig. 3) and d is the diameter of the SWNT. The second form of capacitance is the quantum capacitance denoted by C_Q and expressed by the equation below

$$C_Q = \frac{2e^2}{\hbar v_f} \quad (3)$$

The bundles are deemed to be densely packed, resulting in very weak quantum capacitance between the SWNTs in the bundle [13]. This presumption has also been verified by previous investigations [20, 21].

iii. Resistance

The relationship between the resistance and the length of a SWNT has been theoretically analyzed [18, 19]. The calculations show that the resistance of a ballistic SWNT is dependent on its mean free path and interconnect length as given by the following equation:

$$R = R_b \left(1 + \frac{L}{L_\lambda} \right) \quad (4)$$

where L is the interconnect length, L_λ is the mean free path length, and R_b is the resistance of the ballistic SWNT bundle. The equation for R_b is given below;

$$R_b = \left(\frac{\hbar}{4e^2 n} \right) \quad (5)$$

where n is the number of Nanotubes in the bundle. At the 22 nm node year -which this model is predicated on- L_λ , as estimated will be about $\approx 10\mu\text{m}$ [4].

iv. Conductivity

The conduction of a ballistic SWNT (G) is given by the Landauer formula as shown below;

$$G = \left(\frac{4e^2}{\hbar} \right) T \quad (6)$$

where T is the transmission coefficient of the SWNT, In this work ideal contacts are assumed, whereby $T = 1$, which yields $G = 155 \mu\text{S}$.

B. Cu Transmission Line

The electrical parameters for Cu at the 22 nm node year are more concisely derived from ITRS specifications [22]. Inductance for Cu interconnects is predicted to be $\approx 1 \text{ nH}/\text{mm}$ [23]. The capacitance between adjacent Cu micro-wires can be modeled using the parallel plate capacitance formula given below:

$$C_{Cu} = \left(\frac{\epsilon h_{Cu} l}{d_{adj}} \right) \quad (7)$$

where h_{Cu} is the Cu wire height, l its length and d_{adj} is the separation distance between two adjacent Cu inter-

connects. Resistance per unit length for Cu at the 22 nm node is estimated to be approximately $2.2 \mu\Omega/\text{cm}$.

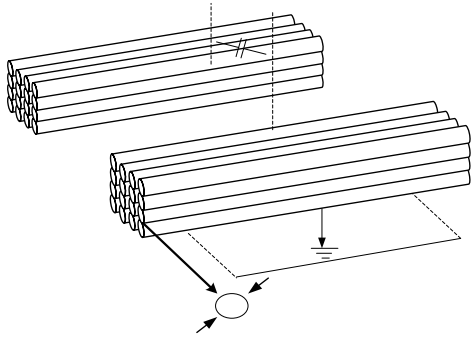


Figure 3: Schematic of adjacent Nanotubes bundle showing their parameters.

The parameters presented in the section provide the basis for a workable RLC model for both the SWNT and Cu micro-wire used to implement the combined scheme for the demultiplexer..

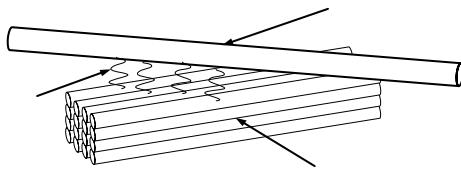


Figure 4: Diagram showing the SWNT-Micro-Wire junction with redundancy of $k = 4$. The redundancies in the bistable molecular junctions are also illustrated.

IV. Demultiplexer Delay Analysis

The introduction of fault-tolerance into the demultiplexer design affects its performance. Using an analog demultiplexer circuit model, which incorporates the NW and Micro-wire RLC transmission line models described earlier, the fault-tolerance induced signal delay is investigated.

The SaberSketch [24] circuit simulator was used to construct and simulate the demultiplexer circuits. Delay measurements were conducted using the Synopsys CosmoScope waveform analysis tool [25]. Delay measurements were made as a function of signal rise-time at the NW address line output.

A $170 \text{ k}\Omega$ resistor was used as the “ON” resistance of the molecular junction; this value is based on empirical data from [26], which indicates a maximum hysteresis current of $10 \times 10^{-6} \text{ A}$ when approximately 1.7 V was applied to the molecular switch junction. The spacing between adjacent interconnect bundles was assumed to be 1 nm or the diameter of a single SWNT. Similar assumptions were made for

the micro-wires. For simplicity, ideal conditions were assumed to eliminate effects resulting from leakage current with unselected SWNTs address line. Hence, all unselected SWNT interconnects were grounded. Each address line consisted of densely packed SWNT bundles, depending on the degree of redundancy implemented. This mitigates effects resulting from parasitic coupling capacitance within the SWNT bundle. The only capacitance given in the model is due to interconnect bundles as discussed in the previous section. The resistance per unit length for each address line SWNT bundle decreases with increasing redundancy; a result of each SWNT in the bundle contributes to conduction.

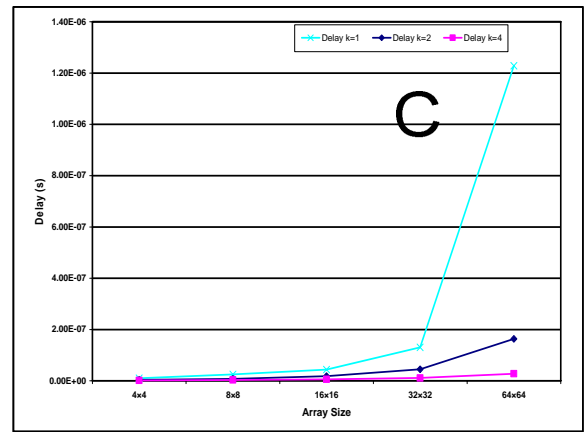


Figure 5: Delay incurred by using redundant SWNT bundles as interconnect address lines.

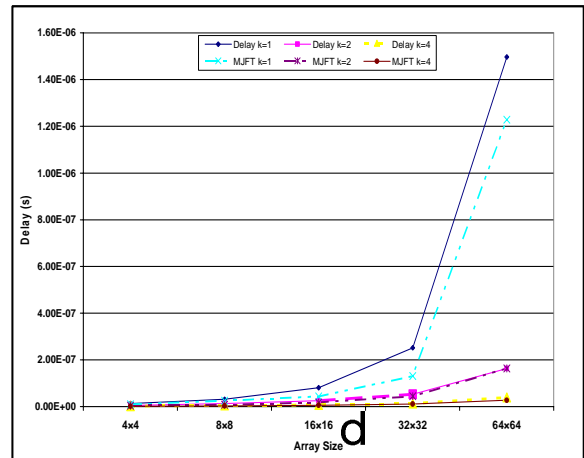


Figure 6: Delay comparison between the multi-junction fault-tolerance scheme and the multi-junction enhanced ECC fault-tolerance scheme.

Redundancies of $k = 1$ (no redundancy), 2, and 4 were implemented in this work. Having $k = 2$, signifies an interconnect bundle that consists of four SWNTs and two molecular switches. The SWNT bundles are stacked vertically in a $k \times k$ geometric configuration.

The delay analysis was based on a worst case lower bound scenario. In other words, the signal delay accrued from selecting the address line output farthest from the driving input signal. All simulations were made under the assumption that every molecular junction functioned correctly. Depending on the degree of redundancy, each junction comprised of k molecular switches in parallel, having a singular connection to the driving micro-scale column wire; Fig 4 illustrates this point.

Results indicate that the inclusion of redundancy at the NW level improves signal delay. This is consistent with projections from recently published works [12, 13, 17]. The delay analysis graph Fig 6, shows better delay improvement with increasing redundancy. The penalty paid by incorporating the molecular switch junction fault-tolerant scheme is manifested primarily through the additional surface area require for implementation. A scale model of the demultiplexer was used in this work; this made it virtually impractical to simulate larger array and redundancy sizes. In the light of the presented result, the molecular switch junction scheme visibly enhances the ECC scheme.

V. Probability Analysis

The probability of yielding a desired number of non-defective molecular switch junctions from a cumulative yield of molecular switches available for a desired SWNT address line is determined using a binomial distribution. Given an address consisting of i bits with $(k - 1)$ redundant bits and x ECC bits, the Binomial (i, p) distribution is the probability of yielding i useable bits from N total bits, given a specified defect probability p . The probability of yielding i non-defective molecular switch junction from N total junctions is given by the following binomial distribution:

$$P_{yield}(N, i) = \left(\binom{N}{i} P^i (1 - P)^{N-i} \right) \quad (8)$$

where, $N = i + (k - 1) + x$.

The binomial coefficient $\binom{N}{i}$ is the number of ways of selecting i good molecular switch junctions from a total of N junctions. For each of these cases, there is a yield probability of $P^i (1 - P)^{N-i}$. Total yield is thus given by the following cumulative distribution equation:

$$P_{MeFN} = \sum_{M \leq i \leq N} \left(\binom{N}{i} P^i (1 - P)^{N-i} \right) \quad (9)$$

The probability analysis assumes an idealized model where defects are uniformly spread with uniform probability and independence. In the probability analysis graph provided in Fig 7, $k = 1$ is considered the benchmark condition; i.e. only ECC is implemented in the demultiplexer. It can be deduced that for lower defect probabilities the molecular switch junction enhanced ECC demultiplexer shows a higher degree of fault-tolerance. At higher defect rates, the ECC only demultiplexer shows a higher degree of fault-tolerance. This is a result of the defect probability weight (binomial coefficient) dominating the process. The defect probability is spread proportionally across each junction; higher redundancies will make the likelihood of making the correct address selection to be dominated by the increase in defect prone junctions. The point where the benchmark case $k = 1$, overtakes the higher redundancies occurs at $p \approx 65\%$.

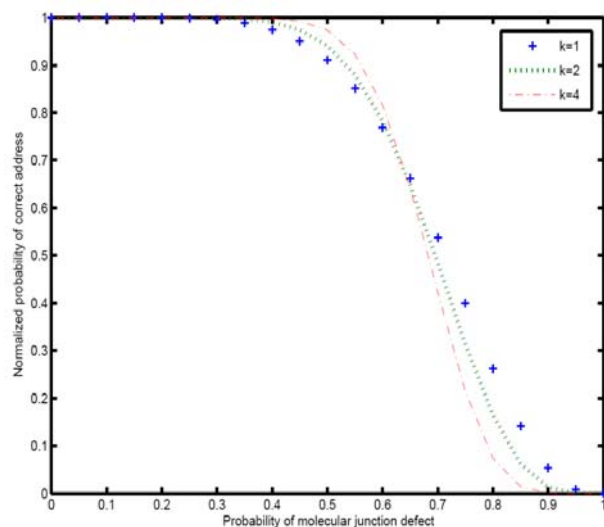


Figure 7: Probability analysis graph showing the normalized probability of selecting the correct input address given range of defects probability. $k = 1$ is the benchmark case indicating an ECC only demultiplexer.

VI. Conclusion

This work has shown that by including redundant SWNT bundles in the AND gate address line of a nanomemory demultiplexer implemented with ECC, delay performance can be further improved. Further, fault-tolerance for the large array of defect probabilities is improved. Utilizing bundles of SWNTs also aid in better signal conduction as it has been shown that single SWNT interconnects possess worse performance metrics than current Cu interconnects. Bundle stacks

are also desirable because they can be densely packed in a vertical geometry.

In future works the multi switch junction enhanced scheme will be implemented in a nanomemory module.

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